

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): An output filter for a delta sigma modulator, comprising:
a first and a second constant current source having first and second outputs, respectively;
a FIR filter having a plurality of delay element arranged in cascade, each element being operative to output data of the delta sigma modulator by controlling currents from the constant current source on the basis of each of the output data to thereby generate a plurality of weighted currents that are weighted according to a filter characteristic, the weighted currents being added separately for inverted and non-inverted signals and outputted separately at an output side of the FIR filter.
2. (previously presented): An output filter for a delta sigma modulator as claimed in Claim 1, further comprising a current-to-voltage conversion unit, said unit having an input side coupled to the output side of the FIR filter and comprising a full differential operational amplifier and feed back resistors, said amplifier having a pair of inputs, each input coupled to a respective one of each separate output of said FIR filter and having an output side .
3. (original): An output filter for a delta sigma modulator as claimed in Claim 2, further comprising a single differential conversion operational amplifier on the output side of the full differential operational amplifier.
4. (original): A digital signal processor comprising an output filter for a delta sigma modulator, as claimed in any of Claim 1 to Claim 3.
5. (previously presented): An output filter for a delta sigma modulator as claimed in Claim 1, wherein each said delay element comprises a flip-flop and a respective pair of MOS transistors.

Amendment under 37 C.F.R. § 1.116
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6. (previously presented): An output filter for a delta sigma modulator as claimed in Claim 5, wherein said flip flop generates two outputs and each said output is coupled to a gate of a respective one of the MOS transistors.

7. (previously presented): An output filter for a delta sigma modulator as claimed in Claim 1, wherein said constant current source comprises a common source for generating said plurality of weighted currents.